DUAL-DIODE LIMITER FOR HIGH-POWER/LOW-SPIKE-LEAKAGE APPLICATIONS

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ABSTRACT

This paper presents procedures, confirmed by both measured data and microwave circuit analysis, for designing dual-diode passive microwave limiters with low spike leakage (less than 100 nJ) and the ability to handle high peak power (on the order of 10 mJ of incident energy). Design parameters covered are diode characteristics, polarity, package parasitics, and the spacing between the diodes. Such limiters are needed to protect sensitive electronics from high-power rf.

INTRODUCTION

Limiter circuits using two silicon PIN diodes have demonstrated significant power handling and spike leakage performance improvements over one-diode limiters [1]. This paper presents a design guide for these dual-diode limiters and describes their analytical and experimental performance. The experimental results are an insertion loss of less than 2 dB up to 8 GHz (limited primarily by the connectors used), high power isolation exceeding 35 dB, and spike leakage less than 70 nJ for incident peak power of 1 kW. Circuits of this type will be required to protect sensitive microwave components, e.g., Monolithic Microwave Integrated Circuit low-noise amplifiers [2].

In this paper two different PIN diode package types were used. One was a pill prong type with an inductance of 0.9 nH and a zero biased junction capacitance of 0.3 pF. The second package was a 50-Ω package designed for use in stripline. This package has a 0.1 nH inductance and a zero bias junction capacitance of 0.15 pF. The results are for those packages using the low-inductance diodes unless specified.

The dual-diode limiters are designed using these diodes placed in shunt across a 50-Ω TEM line as seen in the limiter circuit in figure 1.

DISADVANTAGES OF SINGLE-DIODE SHUNT LIMITERS

A single-diode shunt limiter has three basic limitations. First, because the spike leakage energy and input energy required to damage the PIN diode are both proportional to the intrinsic region (I-region) thickness (see figures. 2 and 3), a high-power limiter with low spike leakage is incompatible with the use of a single diode. Second, the isolation is limited by the diode package inductance, package resistance, and the minimum junction resistance (figure 4 is a circuit model for a packaged PIN diode). Third, a dc return must be used, which limits the bandwidth and adds to the insertion loss. Therefore, two or more diodes must be used in order to handle high input energies and also have low spike leakage energies.

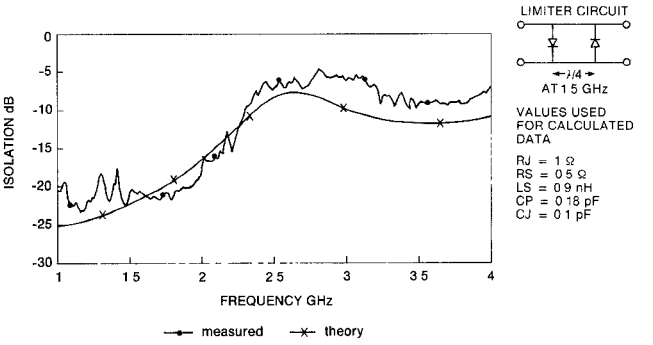

Figure 1. Comparison of calculated and measured insertion loss as a function of frequency for a dual-diode limiter with quarter-wavelength spacing at 1.5 GHz.

DUAL-DIODE LIMITER THEORY

This paper discusses the performance of two-diode limiters which use a thicker I-region diode (with higher reverse breakdown voltage) cascaded with a thinner I-region diode (with lower reverse breakdown voltage). The thicker diode is used in front of the thinner diode to dissipate the high power, while the thinner diode keeps the spike leakage energy low.

The spacing between the diodes affects the insertion loss and the isolation of the limiter. Figure 5 shows s-parameter calculations for two shunt impedances separated by a quarter wavelength at 1 GHz. The isolation for two purely resistive

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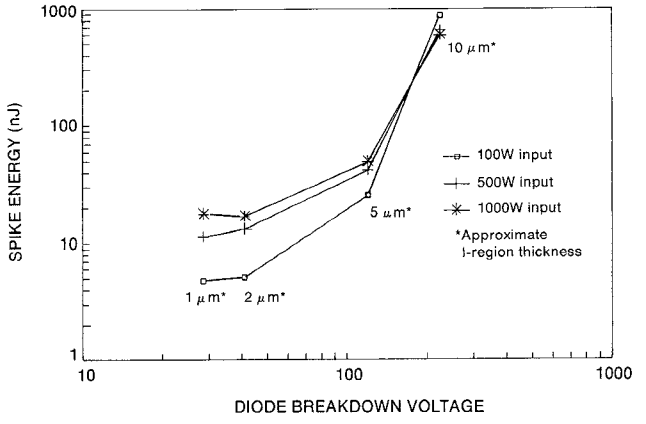


Figure 2. Spike energy increases as diode's reverse breakdown voltage increases (I-region thickness is increased). Data taken at 1.5 GHz.

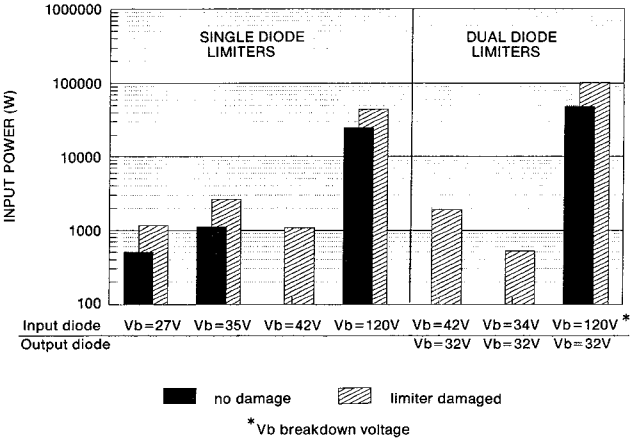
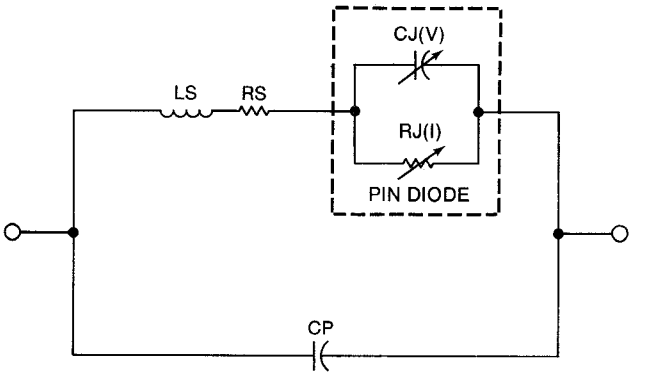


Figure 3. Damage data of seven limiters measured. Reverse breakdown voltages of diodes used are shown under bar graph. Bar graph verifies that damage level of a dual-diode limiter is essentially determined by larger input diode.

elements (L1 = L2 = 0) is maximum at odd multiples of a quarter wavelength. The package inductance of the diode is simulated by using an inductive component (L1 = L2 =0.2 nH). The package inductance shifts the maximum isolation lower in frequency and reduces the isolation obtained as frequency increases.

Figure 1 shows a comparison of analytic results and measured data for a two-diode limiter with both diodes having a 2-μm I-region thickness. In this figure the package inductance of 0.9 nH dominates the response of the limiter. This limiter could not be used much above 2 GHz because of the large diode package inductance.

To design a limiter that will operate at higher frequencies, one must minimize the package parasitics. Filter theory can be used to design a



CJ(V) = JUNCTION CAPACITANCE

RJ(I) = JUNCTION RESISTANCE

RS = SERIES RESISTANCE

LS = SERIES INDUCTANCE

CP = PACKAGE CAPACITANCE

Figure 4. Circuit model for a pill-packaged PIN diode.

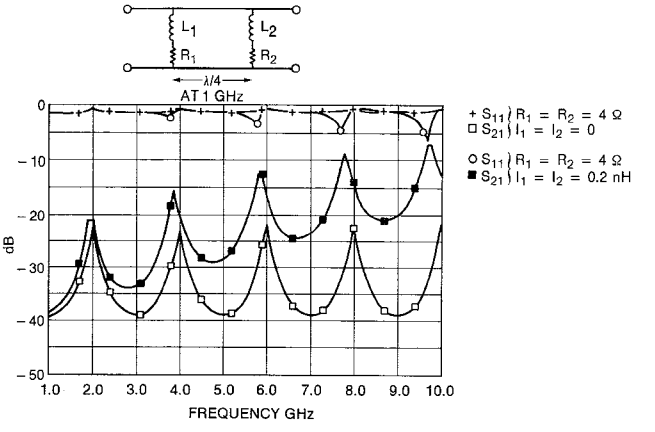


Figure 5. Calculated insertion and return loss as a function of frequency for two shunt impedances separated a quarter wavelength at 1 GHz. Effect of adding inductance is a shift in maxima and a decrease in isolation as frequency increases.

larger bandwidth limiter. The limiter can be designed so that the bond wires and junction capacitance of the diodes are chosen to form an LC low-pass filter structure. Fifty-ohm diode packages are currently available where this technique is used.

Figure 6 shows the measured isolation of a forward-dc-biased, dual-diode limiter using two 2 μm diodes with the 50-Ω packages spaced a quarter wavelength apart at 1.5 GHz. The limiter performs well above the measured 14 GHz. Figure 7 shows the output power plotted as a function of the input power at 1.5 GHz. Isolation is near 40 dB at about 500 W. Comparing the isolation in figure 7 to the maximum isolation regions as a function of frequency

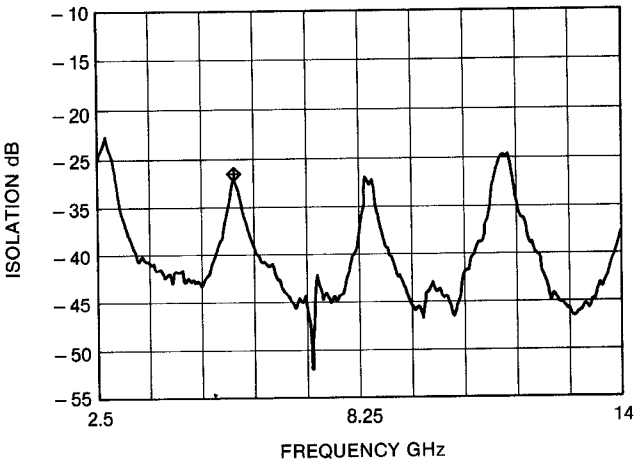


Figure 6. Isolation plotted as a function of frequency for a forward-dc-biased dual-diode limiter using two 2-μm diodes spaced a quarter wavelength apart at 1.5 GHz.

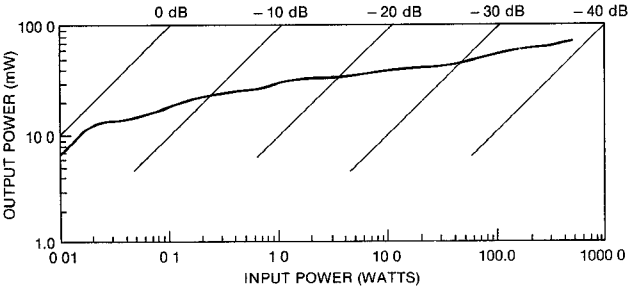


Figure 7. Isolation at 1.5 GHz as a function of input power for a dual-diode limiter using two 2-μm diodes spaced a quarter wavelength apart.

in figure 6 indicates that both diodes are completely turned on with an input of about 500 W.

POWER-HANDLING CAPABILITIES OF DUAL-DIODE LIMITERS

Transmission-line theory was used to determine the distribution of power dissipation of two shunt resistors across a 50-Ω TEM line. Figure 8 shows the percentage of power dissipation as a function of resistor spacing. Resistors r1 and r2 in this plot represent idealized PIN diodes in their on state in a dual-diode limiter. The plot shows that the dissipated power is maximized in the first diode if the diodes are spaced a quarter wavelength apart. The damage level of an idealized dual-diode limiter of this type is essentially determined by the damage level of the diode at the input of the limiter.

Seven limiters (four single diode and three dual-diode limiters) were damage tested. The limiters were subjected to 1 μs pulsewidth, 2.74 GHz microwave pulses at a repetition rate of 10 Hz. The power level was increased in steps of approximately 3 dB until the limiters were damaged. The limiters

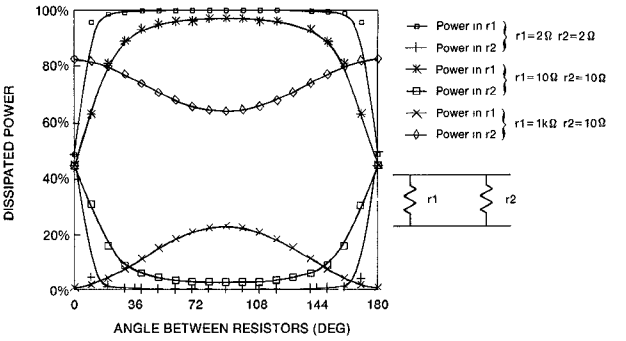


Figure 8. Percentage of dissipated power in two shunt resistors, r1 and r2, in a 50-Ω TEM line, plotted as a function of resistor separation. Dissipated power in r1 is maximized at 90° separation.

were considered damaged when a PIN diode became a short circuit [3].

Figure 3 shows the results of the damage tests. The solid bar indicates the highest power level that the limiter was subjected to without damage. The hashed bar indicates the level at which damage first occurred. Three of the limiters were damaged with the first power level; hence there is no solid bar.

In all the dual-diode limiters, the output diode with a smaller reverse breakdown voltage was not damaged; only the input diode was damaged. The highest power limiter damage tested was a dual-diode limiter using a 5-μm diode (reverse breakdown voltage (Vb) = 120 V) followed a quarter wavelength away by a 1-μm diode (Vb = 32 V), and the damage threshold was found to be greater than 40 kW incident peak power (40 mJ) for a single 1-μs pulse (see figure 2). Higher power limiters could not be damage tested at this frequency and pulse width, because the SMA connectors on the limiters begin to arc at these high incident power levels.

The results of the measurements confirm that the damage level of a dual-diode limiter of this design is determined by the input diode's damage level.

SPIKE LEAKAGE OF DUAL-DIODE LIMITERS

The spike leakage of a dual-diode limiter is a function of the diodes used in the limiter, the order the diodes are placed in the limiter, and the polarity of the diodes. The spike energy is proportional to the diode's reverse breakdown voltage, as seen in the spike energies plotted in figure 2 for single shunt diode limiters with varying breakdown voltages. According to the measured data shown in figure 9, the spike energy in a dual-diode limiter is always less than that of single-diode limiters using the same diodes. The data indicate that the minimum spike leakage is obtained when the diode with the larger reverse breakdown is used at the input. The thinner I-

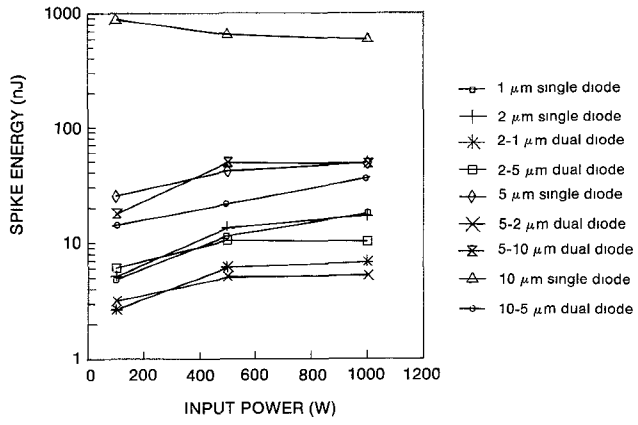


Figure 9. Comparison of spike leakage energy for single- and dual-diode limiters at 1.5 GHz shows that dual-diode limiter with a larger diode followed a quarter wavelength by a smaller diode has less spike leakage than a single-diode limiter using either diode.

region output diode turns on first, and because it is a quarter wavelength away, creates a voltage maximum at the thicker input diode, turning it on faster and thereby reducing the spike leakage energy.

Using the higher inductance pill-packaged diodes, we studied the effect of polarity on spike leakage in dual-diode limiters. The data indicate a reduction in the spike leakage when the diodes are used in opposite polarity. The dc path created when the diodes are in opposite polarity eliminates the need for a dc return, since the current flows in a loop through the two diodes. The rectified current created by the smaller output diode drives the larger input diode into conduction reducing the turn-on time of the limiter, which inturn reduces the spike leakage[4].

CONCLUSION

The information given in this paper can be used to obtain a preliminary design for a dual-diode limiter. The I-region thicknesses of the two diodes are chosen using figures 2 and 3. The thinner diode is chosen according to the spike leakage requirements. The spike leakage in an opposite-polarity dual-diode limiter is essentially determined by the spike leakage of the thinner I-region diode. The thicker I-region diode is chosen to withstand the desired damage level. The diodes should be placed a quarter wavelength apart to maximize both burnout threshold and isolation. The diodes should also be placed with opposite polarities to avoid the need to use a dc return and to minimize spike leakage.

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